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REMARKS

This response, filled with a Request for Continued Examination (RCE) is intended as a full and complete response to the Office Action dated February 24, 2004. In view of the following discussion, the Applicants believe that all claims are in allowable form.

IN THE DRAWINGS

The drawings stand objected to by the Examiner. Specifically, the Examiner asserts that no figure depicts a waveguide clad by the first insulating layer and the top cladding layer as recited in claim 15. The Applicants respectfully disagree. The Application indicates that where the substrate is silicon on insulator, rather than simply silicon, the step of depositing an additional bottom cladding layer is optional. (*Application*, p. 6, ll. 1-10). Thus, the Applicants respectfully submit that one skilled in the art would clearly recognize that the layer 42 deposited in the hole 44 (depicted in figures 4c-f) is optional and may be ignored in the drawings if not deposited. This would result in a waveguide clad by the first insulating layer and the top cladding layer as recited in claim 15.

Additionally, the Examiner asserts that the step of "forming an opening through said semiconductor layer to said first insulating layer and filling said opening with a core material" is not illustrated in the drawings. The Applicants respectfully disagree. As discussed above, the Application discloses that the step of depositing an additional bottom cladding layer is optional. Thus, figures 4a-f and, similarly, figures 5a-h, when taken together with the text of the specification identified above, clearly show every feature of the invention specified in the claims.

Thus, the Applicants respectfully submit that no corrections to the drawings are required. Accordingly, the Applicants request that the objection be withdrawn and the drawings allowed.

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CLAIM REJECTIONS

I. 35 U.S.C. §112 Claims 6-12, 14, 15, and 16-20

Claims 6-12, 14, 15, and 16-20 stand rejected under 35 U.S.C. §112. In response, the Applicants have amended claims 6, 9, and 14 to more clearly recite aspects of the invention. Claim 20 has been cancelled.

Claim 6 has been amended to clarify the core material planarization and silicon oxide and silicon nitride removal steps.

Claim 9 has been amended to positively recite the method step as suggested by the Examiner.

Claim 14 has been amended to correct dependency to claim 13.

The Applicants submit that no new material has been added. Thus, the Applicants submit that claims 6-12, 14, 15, and 16-19 are in allowable form. Accordingly, the Applicants respectfully request that the rejection be withdrawn and the claims allowed.

II. DOUBLE PATENTING Claims 8 and 20

Claim 20 stands provisionally rejected as being a substantial duplicate of claim 8. In response, the Applicants have cancelled claim 20. As such, the Applicants respectfully request that the rejection be withdrawn.

III. 35 U.S.C. §102

A. 35 U.S.C. §102(b) Claims 1-3

Claims 1-3 stand rejected as being anticipated by United States Patent No. 5,877,065, issued March 2, 1999, to *Yallup* (hereinafter *Yallup*). In response, the Applicants have amended claim 1 to more clearly recite aspects of the invention.

Claim 1, as amended, recites limitations not taught or suggested by *Yallup*. *Yallup* does not teach or suggest forming an opening through a semiconductor layer to a first insulating layer then depositing a core material on the first insulating layer to fill the opening, as recited by claim 1. As indicated by the Examiner, the method of *Yallup* requires the deposition of a dielectric layer on the bottom and side walls of the trench

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and then covering the dielectric with a layer of polysilicon. (*Yallup*, figs. 4-7; col. 3, ll. 12-15.) Therefore, *Yallup* does not teach or suggest all of the limitations of independent claim 1 and all claims depending therefrom.

Thus, the Applicants submit that claims 1-3 are patentable over *Yallup*. Accordingly, the Applicants respectfully request the rejection be withdrawn.

B. 35 U.S.C. §102(e) Claims 1, 5, and 9

Claims 1, 5, and 9 stand rejected as being anticipated by United States Patent No. 6,282,358, issued August 28, 2001, to *Hornbeck et al.* (hereinafter *Hornbeck*). The Applicants respectfully disagree.

Claim 1 recites limitations not taught or suggested by *Hornbeck*. *Hornbeck* does not teach or suggest forming an opening through a semiconductor layer to a first insulating layer then depositing a core material on the first insulating layer to fill the opening, as recited by claim 1. Contrary to the assertion of the Examiner, layer 26(a) of *Hornbeck* is a dielectric and not a semiconductor layer. (*Hornbeck*, col. 4, ll. 55-56; col. 6, ll. 57-65.) Furthermore, as indicated by the Examiner, the method of *Hornbeck* requires the deposition of a material such as metal on the side walls and bottom of the trench and then covering the reflective layer with a core material. (*Hornbeck*, figs. 5-10; col. 7, ll. 33-45.) As such, *Hornbeck* does not teach or suggest all of the limitations of independent claim 1 and all claims depending therefrom.

Thus, the Applicants submit that claims 1-3 are patentable over *Hornbeck*. Accordingly, the Applicants respectfully request the rejection be withdrawn.

IV. 35 U.S.C. §103(a)

A. Claims 6-8 and 16-20

Claims 6-8 and 16-20 stand rejected as being unpatentable over *Yallup* in view of publication to Wolf, "Silicon Processing for the VLSI Era," (hereinafter *Wolf*), and further in view of *Hornbeck*. The Applicants respectfully disagree.

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Claim 6 recites limitations not taught or suggested by any combination of the cited references. As discussed above, both *Yallup* and *Hornbeck* fail to teach or suggest etching an opening through a semiconductor layer to a first insulating layer then depositing a core material on the first insulating layer to fill the opening, as recited in claim 6. Thus, *Hornbeck* cannot be utilized to modify *Yallup* to yield a method of forming a waveguide that includes etching an opening through a semiconductor layer to a first insulating layer then depositing a core material on the first insulating layer to fill the opening.

Wolf also does not teach or suggest etching an opening through a semiconductor layer to a first insulating layer then depositing a core material on the first insulating layer to fill the opening, as recited in claim 6. Thus, *Wolf* cannot modify *Yallup* and *Hornbeck* to yield all of the limitations recited in claim 6. As such, a *prima facie* case of obviousness has not been established.

Thus, the Applicants submit that independent claim 6 and claims 7-8 and 16-20 depending therefrom are patentable over *Yallup* in view of *Wolf*, and further in view of *Hornbeck*. Accordingly, the Applicants respectfully request the rejection be withdrawn.

B. Claim 13

Claim 13 stands rejected as being unpatentable over *Yallup* in view of United States Patent No. 6,553,170, issued April 22, 2002, to Zhong et al. (hereinafter *Zhong*). The Applicants respectfully disagree.

As discussed above, claim 1, from which claim 13 depends, recites limitations not taught or suggested by *Yallup*. Specifically, *Yallup* does not teach or suggest forming an opening through a semiconductor layer to a first insulating layer then depositing a core material on the first insulating layer to fill the opening, as recited by claim 1. *Zhong* also does not teach or suggest forming an opening through a semiconductor layer to an underlying first insulating layer, as recited by claim 1. Moreover, *Zhong* does not teach or suggest then depositing a core material on the first insulating layer to fill the opening. Thus, *Zhong* cannot be used to modify *Yallup* in a manner that would yield the invention as recited in claim 1. As such, a *prima facie* case

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of obviousness has not been established since the combination of the cited art fails to teach or suggest all of the limitations recited in claim 1.

Thus, the Applicants submit that claim 13 is patentable over *Yallup* in view of *Zhong*. Accordingly, the Applicants respectfully request the rejection be withdrawn.

C. Claim 14

Claim 14 stands rejected as being unpatentable over *Yallup* in view of United States Patent No. 3,934,061, issued January 20, 1976, to Keck et al. (hereinafter *Keck*). The Applicants respectfully disagree.

As discussed above, claim 1, from which claim 14 depends, recites limitations not taught or suggested by *Yallup*. Specifically, *Yallup* does not teach or suggest forming an opening through a semiconductor layer to a first insulating layer then filling the opening with a core material, as recited by claim 1. *Keck* also does not teach or suggest forming an opening through a semiconductor layer to an underlying first insulating layer, as recited by claim 1. Moreover, *Keck* does not teach or suggest then depositing a core material on the first insulating layer to fill the opening. Thus, *Keck* cannot be used to modify *Yallup* in a manner that would yield the invention as recited in claim 1. As such, a *prima facie* case of obviousness has not been established since the combination of the cited art fails to teach or suggest all of the limitations recited in claim 1.

Thus, the Applicants submit that claim 13 is patentable over *Yallup* in view of *Keck*. Accordingly, the Applicants respectfully request the rejection be withdrawn.

ALLOWABLE CLAIMS

The Applicants thank the Examiner for his comments regarding the allowability of claims 4 and 15 if rewritten in independent form. The Applicants additionally thank the Examiner for his comments regarding the allowability of claims 10-12 if rewritten to overcome the rejections under 35 U.S.C. §112. In response, the Applicants have added claims 21-25, which respectfully recited the limitations of claims 4, 10-12 and 15,

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rewritten in independent form and to overcome the rejections under 35 U.S.C. §112, as suggested by the Examiner.

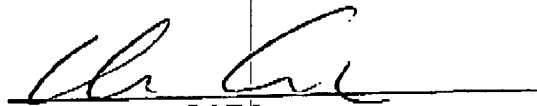
CONCLUSION

Thus, the Applicants submit that all claims now pending are in condition for allowance. Accordingly, both reconsideration of this application and swift passage to issue are earnestly solicited.

If the Examiner believes that any unresolved issues still exist, it is requested that the Examiner telephone Keith Taboada at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

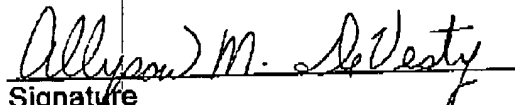
June 21, 2004


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I hereby certify that this correspondence is being transmitted by facsimile under 37 C.F.R. §1.8 on June 21, 2004 and is addressed to Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, Facsimile No: (703) 872-9306.


Signature
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Date of signature